XUSP3S

Xilinx UltraScale 3/4-Length PCIe Board with Quad QSFP, DDR4, QDR-IV, and QDR-II+

- Xilinx Virtex UltraScale 80/95/125/160/190 or Kintex UltraScale 115
- Up to four PCIe x8 interfaces supporting Gen1, Gen2, or Gen3
- Four QSFP28 cages for 1x 400GbE, 4x 100GbE, 4x 40GbE, 16x 25GbE, or 16x 10GbE
- Memory options:
  - up to 64 GBytes of DDR4 SDRAM with ECC
  - up to 36 MBytes QDR-IV
  - Up to 144 MBytes QDR-II+
- Board Management Controller for Intelligent Platform Management
- Timestamping support
- Utility I/O: USB 2.0, serial expansion interface

BittWare's XUSP3S is a 3/4-length PCIe x8 card based on the Xilinx Virtex or Kintex UltraScale FPGA. The high-performance UltraScale devices provide increased system integration, reduced latency, and high bandwidth for systems demanding massive data flow and packet processing. The board offers flexible memory configurations supporting up to 64 GBytes of memory, sophisticated clocking and timing options, and four front panel QSFP cages, each supporting up to 100 Gbps (4x25) - including 100GbE. The XUSP3S also incorporates a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform integration and management. All of these features combine to make the XUSP3S ideal for a wide range of data center applications, including network processing and security, acceleration, storage, broadcast, and SigInt.

Xilinx Virtex or Kintex UltraScale FPGA

The Xilinx UltraScale FPGAs are built on 20 nm process technology and provide ASIC-like clocking for scalability, performance, and lower dynamic power. UltraScale devices are available in two variants: Virtex and Kintex; the XUSP3S board supports both. The Virtex devices feature two types of multi-gigabit transceivers: 32x 16Gb/s (GTH) and 16x 32.75 Gb/s (GTY), while Kintex devices have 48x GTH. The GTY transceivers enable 400GbE, 100GbE, and 25GbE. The Kintex FPGAs support 5,520 DSP slices, while the Virtex supports 1,800. The UltraScale FPGAs provide four integrated blocks for PCI Express, supporting x8 Gen3 Endpoint and Root Port designs. Integrated blocks for 150 Gb/s Interlaken and 100 Gb/s Ethernet (100G MAC/PCS) enable simple, reliable support for Nx100G switch and bridge applications.

I/O Interfaces

The XUSP3S provides a variety of interfaces for high-speed serial I/O as well as debug support. Four QSFP28 cages are available on the front panel, each supporting 100GbE, 40GbE, four 25GbE, or four 10GbE channels, for a total of up to 400 Gbps of bandwidth. The four QSFPs can also be combined for 400GbE. The QSFP channels are connected directly to the UltraScale FPGA via 32 Gb/s GTY transceivers (or GTH for Kintex devices). The QSFP cages can optionally be adapted for SFP+.

Two Gen3 x8 PCIe interfaces connect to the FPGA via 16 GTH transceivers, allowing for a x8 PCIe connection in a standard slot or two x8 interfaces in a bifurcated slot. An optional serial expansion interface on the back side of the board provides a 16x GTH transceiver port connection to the FPGA and can be used to add serial memory, such as Hybrid Memory Cube (HMC). The expansion site can also be used to connect an additional two x8 PCIe interfaces to the FPGA via a cable assembly connecting to an adjacent board that supports PCIe bifurcation, allowing for a total of four x8 PCIe interfaces.

A USB 2.0 interface is available for debug and programming support. The board also supports timestamping with provision for a 1 PPS and reference clock input.

Memory

The XUSP3S features up to 32 GBytes DDR4 on-board as well as two SODIMM sites that support standard DDR4 and proprietary QDR-IV and QDR-II+ SODIMMs. Memory card options include up to 16 GBytes of DDR4 with optional ECC, up to 18 MBytes QDR-IV (1 bank x18 or x36), or up to 72 MBytes QDR-II+ (2 banks x18). Additional on-board memory includes Flash with factory default and support for multiple FPGA images.

Board Management Controller

The XUSP3S features an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I^2C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe or USB. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

FPGA Development Kit

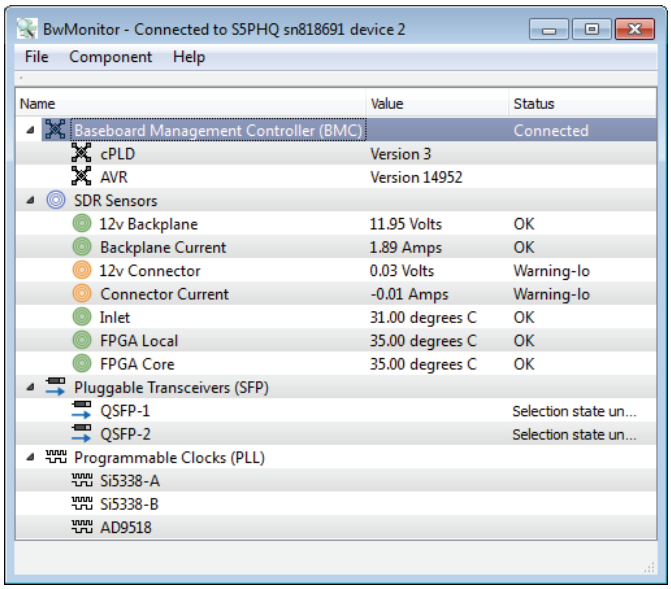
BittWare's FPGA DevKit provides FPGA board support IP and integration for BittWare's FPGA-based boards. The FPGA DevKit includes FPGA components that provide preconfigured physical interfaces, infrastructure, and examples, drastically cutting development time and easily integrating into existing FPGA development environments.

Working example projects are available for each board which illustrate how to move data between the board's different interfaces. Supported interfaces include DDR4, QDR-IV, QDR-II+, PCIe, 10GbE, LVDS, SerDes, and Double Data Rate I/O.

Development Tools

BittWorks II Toolkit

BittWare offers complete software support for the XUSP3S with its BittWorks II software tools. Designed to make developing and debugging applications for BittWare's boards easy and efficient, the Toolkit is a collection of libraries and applications that provides the glue between the host application and the hardware. A variety of features allow developers to take full advantage of the Xilinx UltraScale FPGA capabilities on the BittWare board, including FPGA control via PCIe, Flash programming, custom ISR scripts, and convenient control of FPGA loads. The Toolkit supports 32-bit, and 64-bit Windows and Linux platforms and can connect to the board via PCIe or USB, providing a common API no matter the connection method.



BwMonitor in the BittWorks II Toolkit provides a view into the board management capabilities of your BittWare hardware.

Specifications

Board Specifications

FPGA

- Xilinx UltraScale FPGA
  - Virtex UltraScale 80/95/125/160/190
  - Kintex UltraScale 115
- Multi-gigabit transceivers
  - Virtex: 16x GTY at 32.75 Gbps and 32x GTH at 16 Gbps
  - Kintex: 48x GTH at 16 Gbps
- Up to 1.9 million logic elements
- Up to 132 Mb of embedded memory
- Up to 4 integrated PCIe cores
- Up to 5,520 (Kintex) or 1,800 (Virtex) DSP slices with 27x18 multipliers

On-Board Memory

- Two banks of up to 16 GB DDR4 (x72)
- Flash memory for booting FPGA

Optional SODIMM Memory

- DDR4: x72 w/ECC
  - Up to 16 GBytes per SODIMM
- QDR-IV: x18 or x36
  - Up to 18 MBytes per SODIMM
- QDR-II+ x18
  - Up to 72 MBytes per SODIMM

PCIe Interface

- Two x8 Gen1, Gen2, Gen3 interfaces direct to FPGA (One x8 interface in a standard slot; two x8 interfaces requires bifurcated slot)
- Serial Expansion Port can be used for additional two x8 interfaces

USB Header

- Micro USB port (USB 2.0) for debug and programming FPGA and Flash

QSFP Cages

- 4 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 16 GTY transceivers (GTH for Kintex)
- Each supports 100GbE, 40GbE, 4x 25GbE, or 4x 10GbE (100GbE, 25 GbE Virtex only) and can be combined for 400GbE
- Backward compatible with QSFP and can be optionally adapted for use as SFP+

Serial Expansion Port

- Expansion interface to FPGA via 16x GTH transceivers (optional; requires second slot)

Timestamping

- 1 PPS input
- Reference clock input

Board Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I²C bus access
- USB 2.0 and JTAG access
- Voltage overrides

Size

- 3/4-length, standard-height PCIe slot card
- 241mm x 111.15mm
- Max. component height: 14.47mm single slot, 34.79mm dual slot

Development Tools

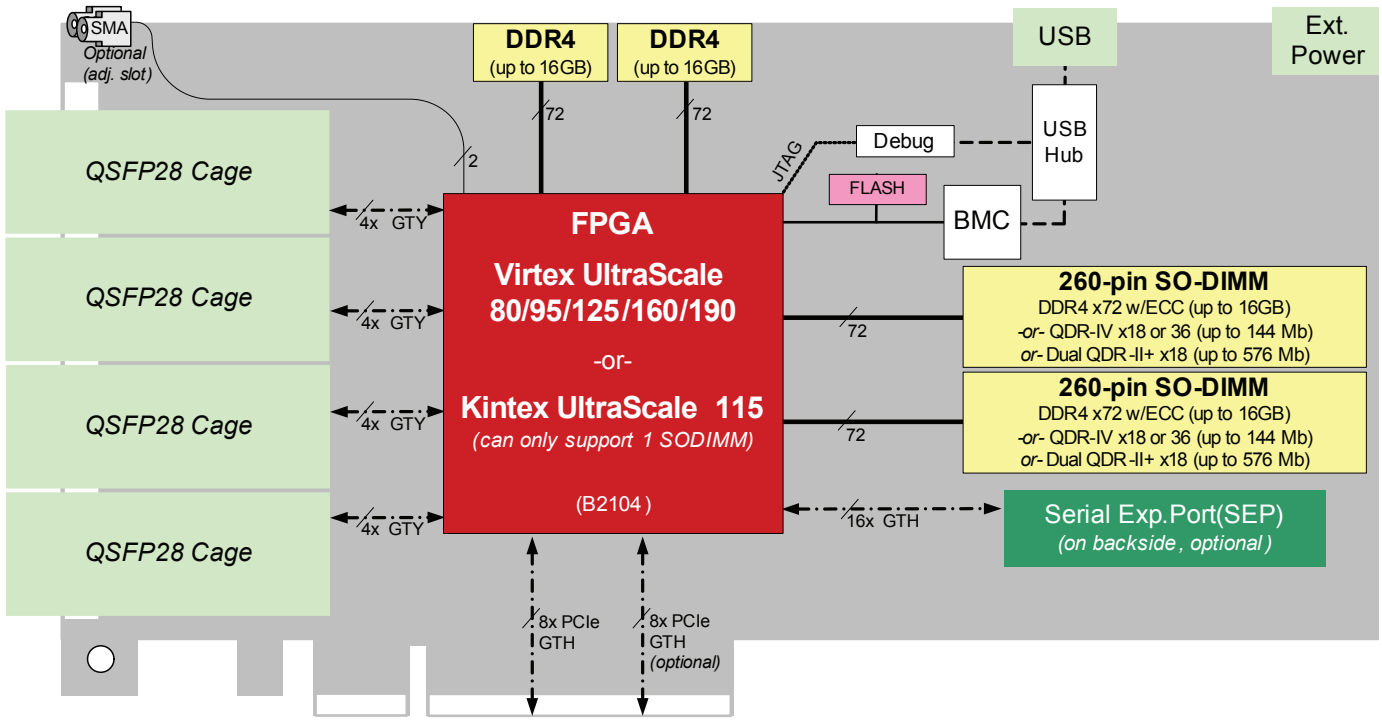
System Development

- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware; Matlab API; source code porting kit also available

FPGA Development

- FPGA Development Kit
  - Physical interface components
  - Board, I/O, and timing constraints
  - Example projects
  - Software components and drivers
- Xilinx Tools
  - Vivado® Design Suite
  - Embedded USB to JTAG converter

Figure 2: XUSP3S System Block Diagram



XUSP3S Ordering Options

XUSP3S - RW-ABBBBCD-EF-GGHH-IJK-LMNOPQ-R

RW	**Ruggedization** 0U = Commercial (0°C to 50°C)*
A	**UltraScale Printed Wiring Board** A = Optimized for 95 FPGA B = Optimized for 125 FPGA*
BBBB	**FPGA Type and Size** 0000 = None 095K = Kintex KU095 095V = Virtex VU095 115K = Kintex KU115 125V = Virtex VU125
C	**FPGA Core Speed Grade** 0 = None 1 = Faster 2 = Nominal* 3 = Slower
D	**FPGA Temperature Range** C = Commercial (Tj = 0 to +85C) E = Extended (Tj = 0 to +100C) I = Industrial (Tj = -40 to +100C)
E	**DDR4 Bank A** 0 = None 2 = 4GB 3 = 8GB 4 = 16GB
F	**DDR4 Bank B** 0 = None 2 = 4GB 3 = 8GB 4 = 16GB
GG	**SODIMM A** 0 0= None E3 = DDR4 8GB x72* E4 = DDR4 16GB x72 Q4 = QDRII+ x18 144Mb Q5 = QDRII+ x18 288Mb
HH	**SODIMM B** 0 0= None E3 = DDR4 8GB x72* E4 = DDR4 16GB x72 Q4 = QDRII+ x18 144Mb Q5 = QDRII+ x18 288Mb
I	**Oscillator** A = Adjustable TCXO T = TCXO
J	**Oscillator Frequency Configuration** 0 = 312.5 MHz fixed
K	**Timing** 0 = None S = Front Panel SMAs X = Onboard Circuits Only
L	**QSFP Configuration** 4 = 4 QSFPs
M	**Serial Expansion Port** 0 = Not Installed 1 = Installed
N	**JTAG** 0 = Not Installed 1 = Installed
O	**USB-to-JTAG** 0 = Not Installed 1 = Installed
P	**Heatsink** 0 = None G = FPGA fansink, single-slot* H = FPGA heatsink, single-slot
Q	**Misc. Configuration** 0 = Default
R	**Assembly** 6 = RoHS 6/6

* Default
† Contact BittWare for availability

DS-XUSP3S | Rev 2015.11.13 | November 2015

BittWare, Inc.
45 South Main Street | Concord, NH 03301 USA
Phone: 603.226.0404
E-mail: info@bittware.com
www.bittware.com/xilinx

BittWare FPGA PLATFORMS