General Standards Corporation

High Performance Bus Interface Solutions

66-18AI32SSC1M

18-Bit, 32-Channel, Differential, 1.0 MSPS, Simultaneous Sampling PMC Analog Input Board

With 1.0 MSPS Sample Rate per Channel and 66 MHz PCI Support

Available in PMC, PCI, cPCI and PC104-*Plus* and PCI Express form factors as:

PMC66-18AI32SSC1M:	**PMC**, Single-width
PCI66-18AI32SSC1M:	**PCI**, short length
cPCI66-18AI32SSC1M:	**cPCI,** 3U
PC104P66-18AI32SSC1M:	**PC104-*Plus***
PCIe66-18AI32SSC1M:	**PCI Express**
PCIe10466-18AI32SSC1M:	**PCIe, one-lane on PC/104 form factor**

See Ordering Information for details.

Call for availability of other form factors, such as XMC, CCPMC, etc.

Features

- **32 Differential Analog Inputs with dedicated 1.0MSPS SAR 18-Bit or 16-Bit ADC per channel. The result is an exceptional combination of precision, throughput and channel density on PMC.**
- **Simultaneous Sampling of all inputs; minimum data skew**
- **Sampling rates from zero to 1.0 MSPS per channel; 32 MSPS aggregate rate**
- **True Differential high-impedance inputs minimize system interference**
- **Input ranges: ±10V or ±5V; software-selectable. ±2.5V or ±1.25V ranges available.**
- **FIFO data buffer stores 512K-Samples of 16-Bit data, or 256K of 18-Bit data**
- **SAR (successive approximation) ADCs provide true simultaneous sampling without a minimum sample rate limitation**
- **D32; 66MHz/33MHz PCI compatibility, with universal 5V/3.3V signaling**
- 2-Channel DMA engine supports both block and demand mode DMA transactions
- Sampling controlled by internal rate generators, by a software trigger, or externally
- Continuous, burst and single-sample clocking modes
- Hardware sync I/O for multiboard operation through both front-panel and internal ports
- On-Demand autocalibration of all channels.
- ***Optional continuous low-drift calibration at lower sample rates.***
- ***Optional internal 20-Bit clock divider for external ADC clock source.***
- Completely software-configurable; No field jumpers
- Single-width PMC form factor with integral EMI shield
- Available with 16-Bit native resolution at reduced cost

Typical Applications

✓ High-Accuracy Analog Inputs	✓ Industrial Robotics	✓ Acoustic Sensor Arrays
✓ Analog Event Capture	✓ Biometric Signal Analysis	✓ Dynamic Test Systems

Rev: 103113

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Functional Description

The PMC66-18AI32SSC1M analog input board samples and digitizes up to 32 input channels simultaneously at rates up to 1,000,000 samples per second for each channel. Native conversion resolution is available as either 18 bits or 16 bits. Data on native 18-Bit boards can be configured as either 16 or 18 bits. Each input channel contains a dedicated successive-approximation (SAR) ADC, the sampled data from which is error-corrected and routed to the PCI bus through a 1-MByte FIFO buffer. The 32-Bit local data path supports full D32 local-bus data packing for 16-Bit data. Throughput performance is further enhanced with 66MHz PCI support. All operational parameters are software configurable.

Inputs can be sampled in groups of 2, 4, 8, 16, or 32 channels, or any contiguous channel group can be designated for acquisition. The sample clock can be generated from an internal rate generator, or by software or external hardware. Input ranges are software-selectable as ±10V or ±5V, or optionally as ±2.5V or ±1.25V. Continuous background calibration can be invoked at lower sample rates.

An on-demand autocalibration feature determines offset and gain correction values for each input channel, and applies the corrections subsequently during acquisition. For low sample rates, below 750SPS, continuous autocalibration can be invoked to minimize both short-term and long-term drift errors. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host.

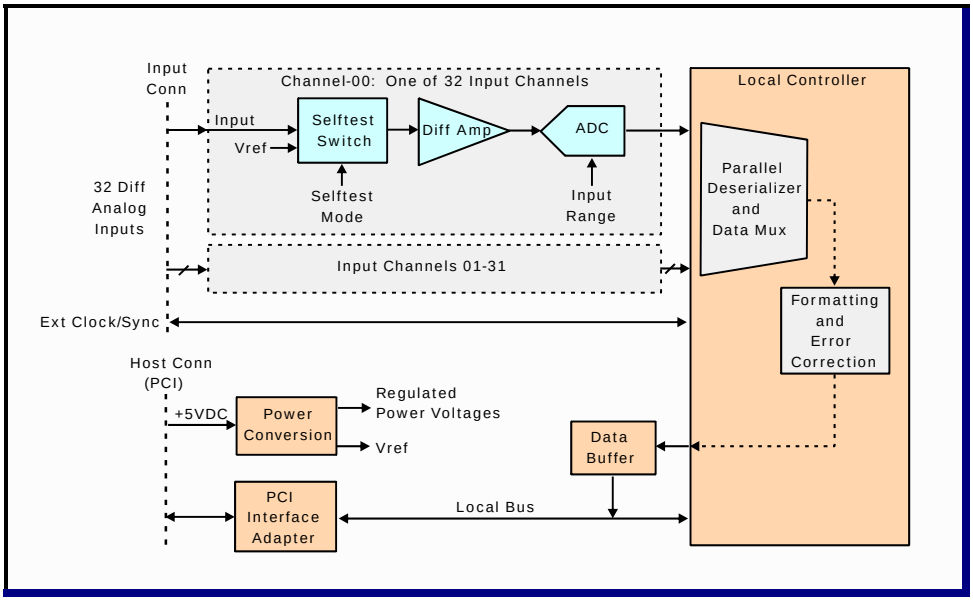

Figure 1. PMC66-18AI32SSC1M; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3. System connections are made through a high-density front-panel I/O connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and operation over the specified temperature range is achieved with standard convection cooling.

Performance Specifications

At +25 ^{O}C, with specified operating conditions.

Input Characteristics:

Configuration:	32 differential analog input channels. Also available with 4, 8 or 16 channels.
Voltage Ranges:	Software configurable as ±10V or ±5V fullscale. Optionally ±2.5V or ±1.25V.
Input Impedance:	2.0 Megohms typical, line-line. 1 Megohm line-ground..
Bias Current:	100 nA maximum
Common Mode Rejection:	60dB typical, DC-50kHz
Maximum Input Voltage	±11V relative to input return, for rated performance. ±6V for the Low-range option.
Crosstalk Rejection:	85dB typical, DC-100kHz
Input Noise:	0.3mVRMS for native 18-Bit configuration; 0.4mVRMS for the 16-Bit configuration; typical *on all ranges.*
Overvoltage Protection:	±30 Volts with power applied; ±15V with power removed.

Transfer Characteristics:

Sample Rate Range:	Zero to 1,000,000 samples per second; all channels simultaneously
Channels per Sample:	1-32.
Input Bandwidth (-3dB):	DC to 800 kHz typical.

	Native 18 Bits	**Native 16 Bits**
Resolution:	18 Bits	16 Bits
DC Accuracy: (Maximum composite error after autocalibration)	Range / Zero-Input / ±Fullscale ±10V ± 0.4mV ± 0.9mV ±5V ± 0.3mV ± 0.6mV ±2.5V* ± 0.2mV ± 0.5mV ±1.25V* ± 0.2mV ± 0.4mV	Range / Zero-Input / ±Fullscale ±10V ± 0.8mV ± 2.0mV ±5V ± 0.6mV ± 1.4mV ±2.5V* ± 0.5mV ± 1.0mV ±1.25V* ± 0.4mV ± 0.8mV
Integral Nonlinearity:	±0.0015 percent of FSR	±0.007 percent of FSR
Differential Nonlinearity:	±0.0008 percent of FSR	±0.004 percent of FSR

* Optional low range set.

Analog Input Operating Modes and Controls:

Input Data Buffer:	1 Megabyte FIFO; 32bits x 256K: 512K-Samples for 16-Bit packed data, or 256K-Samples for 18-Bit data
Input Data Format:	Configurable on native 18-Bit boards as 18 or 16 bits. Nonpacked Mode: 18-Bit or 16-Bit data word plus single-bit Channel-00 tag. 16-Bit data only, on native 16-Bit board. Packed Mode (16-Bit data only): Lword sync code followed by packed channel data, with two data values per Lword.
Data Coding:	Selectable as offset binary or two's complement.
Sample Clock and Sync (trigger) Sources:	Two internal rate generators; External Hardware Clock and Sync I/O, Software clock. Continuous and burst clocking Modes.
Rate Generators:	Programmable from 1,000,000Hz down to 0.01Hz when cascaded. Each generator divides the local master clock through a 16-Bit counter. The standard master clock frequency is 36.000 MHz. See ordering information for custom frequencies.
External Clock and Sync:	Bidirectional TTL lines; Zero to 1.000,000 sample clocks per second. Zero to 250,000 burst triggers per second Available through the I/O connector and through a connector located on the back (Side-2) of the board.
Clock Divider Option:	Optional 20-Bit internal counter supports division of an external ADC clocking source. (Available only for 16-Channel and 32-Channel configurations).

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Autocalibration:

On-Demand Autocal	Calibration of all channels is performed on-demand by a single software command. Acquisition is suspended during on-demand autocalibration, but the calibration can be applied at all sample rates.
Continuous Autocal: (Low-Drift autocal)	Calibration of all channels is performed continuously in the background while the continuous autocal mode is selected, and acquisition is not interrupted. Continuous autocal is effective only at sample rates not exceeding approximately 750 samples per second. Availability of this software-selectable low-drift calibration feature is an ordering option, and does not affect the use of normal on-demand autocalibration .

Physical Parameters

PCI Compatibility:

Conforms to PCI Specification 2.3, with 66MHz/33MHz, D32 and universal signaling (5/3.3 Volt).

Single multifunction interrupt.

DMA transfers in block or demand mode as bus master Two DMA channels available.

Power Requirements:

+5VDC ±0.2 VDC at 1.5 Amps maximum, 1.3 Amps typical.

Maximum Power Dissipation: Side-1: 6.0 Watts. Side 2: 1.5 Watts.

Mechanical Characteristics (PMC Form Factor)

Height: 13.5 mm (0.53 in)
Depth: 143.75 mm (5.66 in)
Width: 74.0 mm (2.91 in)

Environmental Specifications

Ambient Temperature Range:

Standard Temperature:	Operating: 0 to +65 Degrees Celsius inlet air Storage: -40 to +85 Degrees Celsius
Extended Temperature:	Operating: -40 to +80 Degrees Celsius inlet air Storage: -40 to +85 Degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional convection cooling; 150 LFPM

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Ordering Information

Specify the basic product model number followed by an option suffix "**-A-B-C-D-E-F**", as indicated below. For example, model number PMC66-18AI32SSC1M-32-18B-0-0-RevB-CD describes a PMC module with 32 input channels, 18-Bit ADC resolution, standard master clock frequency, ±10V input range set, Low-Drift option, and the clock divider option..

Basic Model Number	Form Factor
PMC66-18AI32SSC1M	PMC (Native)
PCI66-18AI32SSC1M [1]	PCI, short length
cPCI66-18AI32SSC1M [1]	cPCI, 3U
PCIe66-18AI32SSC1M [1]	cPCI, 3U
PC104P66-18AI32SSC1M	PC104-*Plus*
PCIe10466-18AI32SSC1M [1,2]	PCIe, one-lane on PC/104 form factor

[1] Module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

[2] PCIe104 supports only the PCIe bus.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	32 Channels	A = 32
	16 Channels	A = 16
	8 Channels	A = 8
	4 Channels	A = 4
ADC Resolution	18 Bits	B = 18B
	16 Bits	B = 16B
Master Clock Frequency:	36.000 MHz	C = 36M
(Standard frequency is 36 MHz)	Specify custom frequency; (36-40) MHz	C = (Custom frequency)M
Input Range Set:	High set: Selectable as ±10V or ±5V.	D = 10V or '0'
	Low set: Selectable as ±2.5V or ±1.25V.	D = 2.5V
Low Drift Option:	No Low-drift Option	E = NLD
(Continuous autocal)	Low-Drift Option installed	E = LD *
Clock Divider *	20-Bit Divider for external ADC clock source	F = CD **
	No clock divider	F=0

** The low-drift feature is provided on all boards that have a raw-board Revision-B or higher. It is not available on Rev-A boards.*
*** Available only for 32-Channel and 16-channel configuration options ("A" = 32 or 16).*

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Table 1. System I/O Connector

ROW-A			ROW-B	
PIN	SIGNAL		PIN	SIGNAL
1	INP00 LO		1	INP17 LO
2	INP00 HI		2	INP17 HI
3	INP01 LO		3	INP18 LO
4	INP01 HI		4	INP18 HI
5	INP02 LO		5	INP19 LO
6	INP02 HI		6	INP19 HI
7	INP03 LO		7	INP20 LO
8	INP03 HI		8	INP20 HI
9	INP04 LO		9	INP21 LO
10	INP04 HI		10	INP21 HI
11	INP05 LO		11	INPUT RTN
12	INP05 HI		12	INPUT RTN
13	INPUT RTN		13	INP22 LO
14	INPUT RTN		14	INP22 HI
15	INP06 LO		15	INP23 LO
16	INP06 HI		16	INP23 HI
17	INP07 LO		17	INP24 LO
18	INP07 HI		18	INP24 HI
19	INP08 LO		19	INP25 LO
20	INP08 HI		20	INP25 HI
21	INP09 LO		21	INP26 LO
22	INP09 HI		22	INP26 HI
23	INP10 LO		23	INPUT RTN
24	INP10 HI		24	INPUT RTN
25	INP11 LO		25	INP27 LO
26	INP11 HI		26	INP27 HI
27	INPUT RTN		27	INP28 LO
28	INPUT RTN		28	INP28 HI
29	INP12 LO		29	INP29 LO
30	INP12 HI		30	INP29 HI
31	INP13 LO		31	INP30 LO
32	INP13 HI		32	INP30 HI
33	INP14 LO		33	INP31 LO
34	INP14 HI		34	INP31 HI
35	INP15 LO		35	INPUT RTN
36	INP15 HI		36	INPUT RTN
37	INP16 LO		37	DIG RTN
38	INP16 HI		38	CLOCK I/O
39	INPUT RTN		39	DIG RTN
40	INPUT RTN		40	SYNC I/O

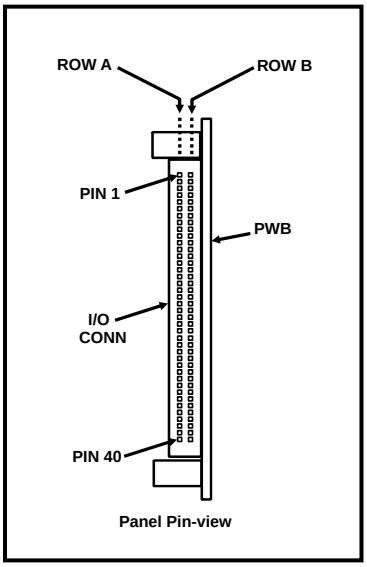

Figure 2. System I/O Connector

System Mating Connector:

Standard 80-pin 0.050" dual-ribbon socket connector:

Robinson Nugent **P50E-080S-TG**
or equivalent.

Table 2. Clock and Sync-I/O Connector

PIN	SIGNAL
1	DIG RTN
2	AUX CLOCK
3	DIG RTN
4	AUX SYNC
5	DIG RTN
6	Reserved. Ground or leave disconnected.

Recommended mating cable connector is Molex# 51146-0600.

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